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EXAMINER	
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2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/785,118	KIMURA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9-13,15-18,23-27 and 29-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-13,15-18,23-27 and 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-4, 9-13, 15-18, 23-27 and 29-32 are pending in the Application.

Claims 1, 9-13, 15, 23-27 and 29-32 have been amended.

Claims 5-8, 14, 19-22 and 28 have been cancelled.

Claims 1-4, 9-13, 15-18, 23-27 and 29-32 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 13 June 2007 in response to the office action mailed on 13 March 2007 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 31 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 31, the limitation, "the bridge module producing address information for two transfer to addresses for the data written to the at least two management modules" renders the claim indefinite. It is clear that said bridge module is used to

produce address information, however it is unclear what is being transferred here (i.e. two transfer to addresses?). Examiner is unclear exactly how address information can be produced for "two transfer to addresses for the data written". Are the addresses of each respective write being transferred, or are the data associated with the addressed produced being transferred?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 32 is rejected under 35 U.S.C. 102(e) as being anticipated by Avraham et al. (US PG Publication 2004/0103238 A1), hereinafter Avraham.

As for claim 32, Avraham teaches a method of efficiently using a mirrored cache, the method comprising:

determining whether a master area of a first memory module is insufficient for a data input request; and storing data initially directed to the master area of a first memory module in a mirror area of a second memory module (paragraph 0054, all lines – Avraham teaches a second memory module as being written with all or part of a first memory module's data once it is determined that the first

memory module is full - paragraph 0054, all lines). Simply stated, Avraham teaches a second memory module as being written with all of part of a first memory module's data once it is determined that the first memory module is full. Note, the data being transmitted from the first memory module to the second was "initially" directed to the master area (i.e. stored there prior to be sent to the second memory).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13, 27, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber (US Patent 5,937,174) in view of Hauck et al. (US PG Publication 2003/0158999 A1), hereinafter Hauck, and in further view of Avraham (US PG Publication 2004/0103238 A1).

As for claims 13, 27, and 30, Weber teaches a storage control apparatus placed between a disk unit and a host for controlling access to said disk unit by said host, said storage control apparatus comprising:

a disk interface module for controlling an interface to said disk unit (Fig. 2, element 138.1);

a host interface module for controlling an interface to said host (Fig. 2, element 204);

Weber further teaches:

a bridge module connected through an interface bus to said disk interface module, said host interface module and said management modules for making connections among said disk interface module (Fig. 2, element 206),

said host interface module and said management modules for data transfer among said modules, said host interface module writing data to be written, which is received from said host, through said bridge module into cache memories of two of said plurality of management modules (referring again to Fig. 2, the host can communicate with the storage module (element 104, which contains multiple modules or drives) via the host interface, the bridge and the disk interfaces (elements 204, 206, and 138.1 respectively)) - col. 7, line 47 through col. 8, lines 39. It is worthy to note that even though Weber teaches storing in the disks rather than the cache, an obvious variation of Weber's apparatus would include Hauck's storage system, as will be discussed *infra*.

Though Weber teaches multiple management modules (disks (106) within the disk storage system (104)), he fails to teach said modules containing cache used to mirror data.

Hauck however teaches an apparatus for maintaining cache coherency in a storage system, which includes a storage system (Fig. 1, elements 110, 112 ... 118, 120, 130 and 160) including a plurality of control units (Fig. 1, element 110, 112, ...

118). Referring to Fig. 2, each control unit (i.e. controller) contains a Read Write Cache Area, and a Cache Copy Area – paragraph 0039, all lines. Since Hauck's controllers inherently controller access to the storage system, they assert at least some control over the control system.

Weber additionally fails to teach the management modules as containing cache with the ability to mirror data, however Hauck teaches each of said management modules including management means (each controller is used to manage read/write functions to the cache) for managing information on the management module which is in mirror relation to this management module (referring to Fig. 2, Host Write #1 data (230) is written to controller 2 (i.e. mirrored), and likewise Host Write #2 data (270) is mirrored to controller 1 – paragraph 0039-0040 all lines). Hauck additionally teaches managing the association between a master area address in said cache memory in this management module and a mirror area address in said cache memory of the management module being in the mirror relation to this management module (referring to Fig. 4, a master area for each cache is maintained (Read/Write/Copy Cache)). The controllers maintain cache coherency by transmitting and receiving metadata, which comprise a bit map and cache identifier. These data allows the controllers to maintain their respective hash tables (Fig. 4, elements 490 and 495) which allows the controllers to maintain where cache lines are present in the cache area, and also maintain a free list of mirror locations (paragraphs 0045-0048, all lines).

Hauck additionally teaches in a case in which a capacity of a master area of said cache memory of the one second module is full when data read out from said disk unit

through said disk interface module and said bridge module is temporarily preserved in the cache memory of the one second management module, the one second management module preserves the readout data in a mirror area of said cache memory of the other second management module, which is in the mirror relation to this management module, on the basis of a situation of management by said management means (Hauck discusses the system's ability to preserve data by reading out the data from a survivor controller (referring to Fig. 7, element 710) and reading into a replacement controller (730) to preserve data that was stored in the failed controller (720). This process takes place in case of a controller failure, or if a large ownership of data is shouldered by the controller (i.e. cache becomes full) – paragraph 0054-0056, all lines).

Lastly, neither Hauck nor Weber teach a master area of said one second module and a mirror area of said other second module are written to until the master area of said one second module is full, at which time a mirror area of said one second module are written.

Avraham however teaches an appliance including a FLASH memory in which a second memory module is written with all or part of a first memory module's data once it is determined that the first memory module is full (paragraph 0054, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly

through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Avraham's appliance including a FLASH memory in to his own scalable memory. By doing so, Weber would have a more robust memory system, capable of increasing the efficiency and reducing wear in case of a catastrophic system failure as taught by Avraham in paragraphs 0005 through 0006, all lines.

6. Claims 1-4, 9-12, 15-18, 23-26, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Weber (US Patent 5,937,174), Hauck (US PG Publication 2003/0158999 A1), and Avraham (US PG Publication 2004/0103238 A1), and in further view of Hashimoto et al. (US PG Publication 2002/0016898 A1), hereinafter Hashimoto.

As for claims 1, 15, and 29, Weber teaches a storage control apparatus placed between a disk unit and a host for controlling access to said disk unit by said host, said storage control apparatus comprising:

a disk interface module for controlling an interface to said disk unit (Fig. 2, element 138.1);

a host interface module for controlling an interface to said host (Fig. 2, element 204);

Weber further teaches:

a bridge module connected through an interface bus to said disk interface module, said host interface module and said management modules for making connections among said disk interface module, said host interface module and said management modules for data transfer among said modules (Fig. 2, element 206),

said bridge module including:

address production means for analyzing said addressing information, which is received together with said data to be written from said host interface module, to produce two transferred-to addresses for designation of said two management modules having said cache memories in which said data is to be actually written and to produce written-in addresses in said cache memories (col. 8, lines 20-39) – the bridge unit works in conjunction with the host interface and the memory controller. The bridge unit receives data and address from the host interface and memory controller in order to communicate with (i.e. perform

memory access functions on) the memory subsystem. The interface and memory controller help to permit the bridge to get the correct data to the correct locations on the disks within the subsystem; and

data transfer control means for controlling data transfer from said bridge module to said management modules so that, after said data is transferred to the two management modules corresponding to said two transferred-to addresses, said data is written at said written-in address in said cache memory of each of the two management modules (Fig. 2, the host (108) can write and read data to and from the storage system via the host interface (204) to the bridge (206), through the device interface (138.1) – col. 7, line 47 through col. 8, lines 39). Again, it is worthy to note that even though Weber teaches storing in the disks rather than the cache, an obvious variation of Weber's apparatus would include Hauck's storage system, as per the discussion *supra* (per claims 13 and 27). When the host writes to the storage system, the data is mirrored in Hauck's system such that at least two addresses (one for each controller's cache) are written-in to.

Weber additionally teaches one of the two management modules as including management means for managing information on the management module which is in mirror relation to the other management module and for managing the association between a master area address in said cache memory of the one second management module and a mirror area address in said cache memory of the other second management module being in the mirror relation to this management module - referring

to Fig. 2, host write 1 data (230) is written to controller 2 (i.e. mirrored), and likewise host write data 2 (270) is mirrored to controller 1 – paragraph 0039-0040 all lines. Additionally, Weber teaches (referring to Fig. 4) a master area for each cache is maintained (Read/Write/Copy Cache). The controllers maintain cache coherency by transmitting and receiving metadata, which comprise a bit map and cache identifier. These data allows the controllers to maintain their respective hash tables (Fig. 4, elements 490 and 495) which allows the controllers to maintain where cache lines are present in the cache area, and also maintain a free list of mirror locations (paragraphs 0045-0048, all lines).

Though Weber teaches multiple management modules (disks (106) within the disk storage system (104)), he fails to teach said modules containing cache used to mirror data.

Hauck however teaches an apparatus for maintaining cache coherency in a storage system, which includes a storage system (Fig. 1, elements 110, 112 ... 118, 120, 130 and 160) including a plurality of control units (Fig. 1, element 110, 112, ... 118). Referring to Fig. 2, each control unit (i.e. controller) contains a cache area (270), and a cache copy area (280) – paragraph 0039, all lines. Since Hauck's controllers inherently controller access to the storage system, they assert at least some control over the control system.

Neither Hauck nor Weber teach a master area of said one second module and a mirror area of said other second module are written to until the master area of said one

second module is full, at which time a mirror area of said one second module are written.

Avraham however teaches an appliance including a FLASH memory in which a second memory module is written with all or part of a first memory module's data once it is determined that the first memory module is full (paragraph 0054, all lines).

Lastly, neither Weber nor Hauck nor Avraham teach the host interface as generating the address to select where data is to be written.

Hashimoto however teaches a host interface circuit in which a host interface device (Fig. 3, element 103) has the ability to generate two unique address via the address generating circuit (206a), which uses two pointers to help generate the addresses (paragraph 0064, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Avraham's appliance including a FLASH memory

in to his own scalable memory. By doing so, Weber would have a more robust memory system, capable of increasing the efficiency and reducing wear in case of a catastrophic system failure as taught by Avraham in paragraphs 0005 through 0006, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further incorporate Hashimoto's host interface device into his own memory structure for high data bandwidth RAID applications. By doing so, Weber would have a more efficient means of interfacing from his host to bridge unit, which includes reducing the power consumption caused by excessive signal transition on the address bus as taught by Hashimoto in paragraphs 0013 and 0017, all lines.

As for claims 2-3 and 16-17, Hashimoto further teaches designating, in said addressing information, a page address in said cache memory of each of said management modules and an offset address in a page designated by said page address, as said written-in address for said data in said cache memory, and specific information for specifying said two management modules having said cache memories in which said data is to be actually written, as said two transferred-to addresses for said data (Hashimoto discusses address conversion circuitry for both the first and second addresses. The address conversion circuitry uses the generated address and an offset (inherent for the conversion to take place) to generate appropriate addresses, in order to access the memories, paragraph 0019-0020, all lines).

As for claims 4 and 18, Weber teaches interface bus is a PCI (Peripheral Component Interconnect) bus, and numbers for specifying said PCI bus for said two management modules are designated as said specific information (col. 8, lines 20-39).

It is worthy to note that since Weber only teaches one bus line, the addresses generated by Hashimoto could only refer to the one address bus that is used to transfer the data specified by the generated addresses.

Again, it would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further incorporate Hashimoto's host interface device into his own memory structure for high data bandwidth RAID applications. By doing so, Weber would have a more efficient means of interfacing from his host to bridge unit, which includes reducing the power consumption caused by excessive signal transition on the address bus as taught by Hashimoto in paragraphs 0013 and 0017, all lines.

As for claims 9-12 and 23-26, Hauck teaches a case in which a capacity of a master area of said cache memory is full when data read out from said disk unit through said disk interface module and said bridge module is temporarily preserved in the cache memory, each of said management modules preserves the readout data in a mirror area of said cache memory of the management module, which is in the mirror relation to this management module, on the basis of a situation of management by said management means (Hauck discusses the system's ability to preserve data by reading out the data from a survivor controller (referring to Fig. 7, element 710) and reading into a replacement controller (730) to preserve data that was stored in the failed controller (720). This process takes place in case of a controller failure, or if a large ownership of data is shouldered by the controller (i.e. cache becomes full) – paragraph 0054-0056, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

Response to Arguments

7. Applicant's arguments have been fully considered however they are not persuasive.

8. Under the heading, "REJECTIONS under 35 U.S.C. § 102", Applicant asserts, "Avraham discusses copying data from the volatile memory to the non-volatile memory when the volatile memory is full. It does not teach or suggest redirecting the storing from the master of the first module to the mirror of the second when the master area of the first memory module is full. Therefore, Avraham does not teach or suggest "storing data initially directed to the master area of a first memory module in a mirror area of a second memory module," as in amended claim 32."

This argument however is not persuasive, as it is not commensurate with the scope of the instant claim. For example, presently amended claim 32 does not require

"**redirecting** the storing from the master of the first module to the mirror of the second when the master area of the first memory module is full" (emphasis added) as alleged by Applicant. The claim requires, *inter alia*, "storing data initially directed to the master area of a first memory module in a mirror area of a second memory module". As discussed in the rejection of claim 32, *supra*, Avraham teaches a second memory module as being written with all of part of a first memory module's data once it is determined that the first memory module is full – paragraph 0054, all lines. Since the data being transmitted from the first memory module to the second was "initially" directed to the master area (i.e. stored there prior to be sent to the second memory), Avraham does in fact anticipate the instant claim in present form, Applicant's arguments notwithstanding.

9. Under the heading, "REJECTIONS under 35 U.S.C. § 103" (claims 13, 27 and 30), Applicant asserts, "Avraham does not teach or suggest redirecting the storing from the master of the first module to the mirror of the second when the master area of the first memory module is full. Therefore, it does not teach "a master area of said one second module and a mirror area of said other second module are written to until the master area of said one second module is full, at which time a mirror area of said one second module are written," as in amended claims 13, 27 and 30."

Again this argument is not persuasive for similar reasons as stated above with respect to the arguments under § 102. More specifically, Avraham does in fact teach writing to a mirror area of a second module when the master area of a first module is

full, therefore Examiner maintains that Weber in view of Hauck, and in further view of Avraham do in fact render these claim obvious.

Applicant further attempts to assert non-obviousness by alleging that the combination of Avraham's FLASH and Hauck's redundant controller "servers [sic] no purpose and thus, the references teach away from combination". Applicant further contends "as the combination serves no purpose, the added cost of FLASH memory would make the resulting combination more expensive".

This argument again is not persuasive. First it is worthy to note that the rejections of claims 13, 27 and 30 were rendered obvious over Weber in view of Hauck, and in further view of Avraham, not Hauck in view of Avraham as suggested by Applicant's argument. Applicant failed to address whether or not Weber in view of Hack and in further of Avraham render the claim obvious, as asserted by Examiner in the previous and present rejections of these instant claims. Applicant's allegation that two of the three cited references may teach away from their combination is therefore not persuasive, since they are not sufficient to rebut Examiner's *prima facie* case of obviousness. Lastly, Applicant's argument with respect to the cost effectiveness of the combination is not persuasive. Applicant is reminded, pursuant to MPEP § 2145, subsection VII. "[t]he fact that a combination would not be made by businessmen for economic reasons does not mean that a person of ordinary skill in the art would not make the combination because of some technological incompatibility. *In re Farrenkopf*, 713 F.2d 714, 219 USPQ 1 (Fed. Cir. 1983)".

Applicant further asserts (page 14 of Applicant's remarks), "the present claims discuss writing to a master area of a cache and the mirror area of a different cache and only when the master area of the first cache is full starting writing in the master area of a second cache. Therefore, Hauck does not teach a "capacity of a master area of said cache memory of the one second module is full when data to be read out through said bridge module into said first module is temporarily preserved in the cache memory of the one second module ...".

This argument however is not persuasive, as it is not commensurate with the scope of the instant claims. For example, presently amended claim 30 does not require "writing to a master area of a cache and the mirror area of a different cache and **only** when the master area of the first cache is full starting writing in the master area of a second cache" (emphasis added) as alleged by Applicant. The claim requires, *inter alia*, "capacity of a master area of said cache memory of the one second module is full when data to be read out through said bridge module into said first module is temporarily preserved in the cache memory of the one second module". Referring again to Hauck, Fig. 7 – the survivor controller (710) reads data from one controller (for example 720) and stores it in the replacement controller (730). This process occurs in case of a controller failure or if a large ownership of data is shouldered by one particular controller (i.e. cache of that particular controller becomes full).

10. Under the heading, "REJECTIONS under 35 U.S.C. § 103" (claims 1-4, 9-12, 15-18, 23-26 and 29), Applicant asserts "Hashimoto paragraph 0064 discusses generation of two specific addresses used for continuous access to a series of areas, it is not

writing to two mirrored cache areas. Therefore, Hashimoto does not disclose "address production means for analyzing said addressing information, which is received together with said data to be written from said first module, to produce two transferred-to addresses for designation of said two second modules having said cache memories in which said data is to be actually written and to produce written-in addresses in said cache memories," of claim 1."

This argument however is not persuasive. Referring to page 11 (final eight lines) of the previous Office action, it is Weber (not Hashimoto as suggested by Applicant) that teaches this limitation. It is worthy to note that Examiner's relies on Hashimoto in the previous Office action (please refer to page 14, lines 6-9), however the Hashimoto reference is relied upon in an § 103 rejection asserting obviousness over the combined teachings of Weber, Hauck and Avraham, in further view of Hashimoto. Applicant's attempt to assert non-obvious by attacking a single reference in the rejection is not persuasive. More specifically, pursuant to MPEP § 2145, subsection IV., "One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)."

Applicant additionally asserts, "nothing cited or found in Hauck suggests a master area of a cache memory. While the present claims have a mirror area, the mirror area is not analogous to the master area, and therefore, Hauck does not teach "wherein, in a case in which a capacity of a master area of said cache memory of the one second module is full when data to be read out through said bridge module into

said first module is temporarily preserved in the cache memory of the one second module, the one second module preserves the readout data in a mirror area of said cache memory of the other second module on the basis of a situation of management by said management means," as recited in claim 9."

This argument however is not persuasive. Hauck does in fact teach master and mirror areas of cache memories, Applicant's arguments notwithstanding. For example (referring to Figs. 2 and 7), each controller contains an area for host data (i.e. master – element 230 for example), and a mirrored area (the copy cache area of element 210 possesses mirror host write #2 data). Fig. 7 further depicts each controller as having a primary area of cache and a mirrored area.

11. Under the heading, "REJECTIONS under 35 U.S.C. § 103" (claims 4 and 18), Applicant alleges, "Examiner admits that the combination of Weber and Hashimoto do not teach or suggest numbers specifying the PCI bus for each bus. Therefore, Weber, Hauck, Avraham and Hashimoto fail to teach or suggest "wherein said interface bus is a PCI (Peripheral Component Interconnect) bus, and numbers for specifying said PCI bus for said two second modules are designated as said specific information," as in claims 4 and 18."

This argument however is not persuasive. Examiner clearly asserts in the final three lines of page 15 of the previous Office action that Weber in fact teaches this very limitation. Applicant clearly misconstrued Examiner's explanation in the following lines as an admission that the previously cited references fail to teach said limitation. The claim in present form requires "a PCI bus", which Weber clearly teaches, as previously

asserted by Examiner (please refer to Fig. 2 and col. 8, lines 20-39).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

13. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
7/27/07